

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 04-328874

(43)Date of publication of application : 17.11.1992

(51)Int.Cl.

H01L 29/804

H01L 21/20

H01L 29/04

(21)Application number : 03-124862

(71)Applicant : SANYO ELECTRIC CO LTD

(22)Date of filing : 27.04.1991

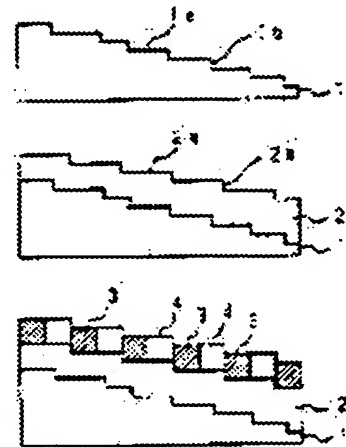
(72)Inventor : TERADA SATOSHI

## (54) ELECTROSTATIC INDUCTION TRANSISTOR AND MANUFACTURE THEREOF

### (57)Abstract:

**PURPOSE:** To obtain a grid and a channel section possessed of a hetero-junction interface excellent in Schottky junction characteristics.

**CONSTITUTION:** A substrate 1 has such a stepped and sloping surface that flat terraces 1a and steps 1b whose risers are vertical to the terraces 1a are provided extending from one side to the other side, and an N-type GaAs semiconductor layer 2 is provided onto the surface of the substrate 1 to form terraces 2a and steps 2b uniform in shape, a vertical superlattice layer which constitutes a grid section 3 and a vertical superlattice layer which forms a channel section 4 are formed on each of the terraces 2a through an atomic layer epitaxy method taking advantage of the steps 2b so as to come into contact with each other, and an I-type GaAs semiconductor layer 5 is laminated thereon.



## LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]